IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. **RA043D2C3C2**)

In the Application of:	)	
	)	
FARMWALD ET AL.	)	**Group Art Unit:** 2818
	)	
Serial No: 09/779,296	)	**Before**
	)	**Examiner:** T. Nguyen
Filed: February 8, 2001	)	
	)	
Title: MEMORY DEVICE HAVING A VARIABLE DATA OUTPUT LENGTH	)	

4/IDS
S Markey
7-7-01

Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

DUPLICATE

The documents listed in the PTO-1449 are documents which were cited and provided in a parent application of the above-referenced application, namely Application Serial No. 09/492,982, filed January 27, 2000. Pursuant to 37 C.F.R. §1.98(d) and M.P.E.P. §609, copies of the documents listed in the modified Form PTO-1449 are not provided herewith.

It is believed that the Examiner may find the documents cited in the modified Form PTO-1449 material to the patentability of one or more of the claims in the above-captioned application. Accordingly, it is respectfully requested that the Examiner make his consideration of these references formally of record with the initial Office Action.

Respectfully submitted,

Date: May 1, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,570,220	02/11/86	Tetrick et al.			
	4,099,231	07/04/78	Kotok et al.			
	5,175,835	12/29/92	Beighe et al.			
	4,937,734	06/26/90	Bechtolsheim			
	4,825,416	05/25/89	Tam			
	5,083,296	01/21/92	Hara et al.			
	4,792,926	12/20/88	Roberts			
	4,953,128	08/28/90	Kawai et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	D. Kawley, "SUPERFAST BUS SUPPORTS SUPERFAST TRANSACTIONS", High Performance Systems, pp 90-94 (Sept. 89)
	H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC", IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990)
	S. Watanabe et. al., "AN Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial READ/WRITE Mode", IEEE Journal of Solid State Circuits, vol. 24 No. 3, pp. 763-770 (June 1982)
	D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5-μm Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988)
	T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,445,204	04/24/84	Nishiguchi			
	4,821,226	04/11/89	Christopher et al.			
	4,882,712	11/21/89	Ohno et. al.			
	4,951,251	08/21/90	Yamaguchi et al.			
	4,928,265	12/29/92	Beighe et al.			
	5,107,465	04/21/92	Fung et al.			
	5,206,833	04/27/93	Lee			
	4,953,128	08/28/90	Kawai et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	T.L. Jeremiah et. al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul,. Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982)
	L. R. Metzeger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562-567 (Oct. 1983)
	A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989)
	D. Jones, "Synchronous static ram", Electronics and Wireless World, vol.93, no.1622, pp. 1243-4 (Dec. 87)
	K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990)
	F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989)
	M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference

EXAMINER	DATE CONSIDERED
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	5,140,688	08/18/92	White et al.			
	5,018,111	05/21/91	Madland			
	4,734,880	03/29/88	Collins			
	4,183,095	01/08/80	Ward			
	4,975,872	12/04/90	Zaiki			
	5,016,226	05/14/91	Hiwada et al.			
	5,109,498	04/28/92	Kamiya et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	D. Wendell et. al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990)
	R. Schmidt, "A memory Control Chip fo Formatting Data into Blocks Suitable for Video Applications", IEEE Transactions on Circuits and Systems, vol. 36, No. 10 (Oct. 1989)
	D. K. Morgan "The CVAX CMCTL – A CMOS Memory Controller Chip", Digital Technical Journal, No. 7 (Aug. 1988)
	T.C. Poon et. al., "A CMOS DRAM-Controller Chip Implementation", IEEE Journal of Solid State Circuits, vol. 22 No. 3, pp. 491-494 (June 1987)
	E.H. Frank "The SBUS: Sun's High Performance System Bus for RISC Workstations" Sun Microsystems Inc. 1990

EXAMINER	DATE CONSIDERED
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,205,373	May 27, 1980	Shah et al.			
	4,845,670	Jul. 4, 1989	Nishimoto et al.			
	4,509,142	Apr. 2, 1985	Childers			
	4,685,088	Aug. 4, 1987	Ianucci			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
	0 246 767	April 28, 1987	EPO				
	0 334 552	Mar. 16, 1989	EPO				
	0 276 871	Jan. 25, 1988	EPO				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	European Search Report for EPO Patent Application No. 00 101 1832
	European Search Report for EPO Patent Application No. 89 30 2613
	Z. Arnitai, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Mico Northeast: Focusing on the OEM Conference Record, pp. 1132, 4/31-3, (April 1987)
	N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986)
	H. Kuriyama et al., "A 4-Mbit CMOS SRAM WITH 8-NS SERIAL ACCESS TIME" , IEEE Symposium On VLSI Circuits Digest Of Technical Papers, pp. 51-52, (June 1990)
	J. Chun et al., "A 1.2ns GaAs 4K Read Only Memory", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 83-86, (Nov. 1988)
	A. Fielder et al., "A 3 NS 1K X 4 STATIC SELF-TIMED GaAs RAM", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 67-70, (Nov. 1988)
	JEDEC Standard No. 21C

EXAMINER	DATE CONSIDERED
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified)	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,945,516	07/31/90	Kashiyama			
	4,807,189	02/21/89	Pinkham et al.			
	4,586,167	04/21/89	Fujishima et al.			
	4,337,523	06/29/82	Hotta et al.			
	4,920,483	04/24/90	Pogue et al.			
	4,845,664	07/04/89	Aichelmann, Jr. et al.			
	4,750,839	06/14/88	Wang et al.			
	4,513,370	04/23/85	Ziv et al.			
	4,975,872	12/04/90	Zaiki			
	5,109,498	04/28/92	Kamiya et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	F. Miller et. al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", Midcon/87 Conference Record, pp. 430-432 Chicago, IL, USA; 15-17 Sept. 1987
	K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,891,791	01/02/90	Iijima			
	4,092,665	05/30/78	Saran			
	4,799,199	01/17/89	Scales, III et al.			
	5,093,807	03/03/92	Hashimoto et al.			
	3,882,470	05/06/75	Hunter			
	4,315,308	02/09/82	Jackson			
	5,148,523	09/15/92	Harlin et al.			
	5,142,637	09/25/92	Harlin et al.			
	4,719,602	01/12/98	Hag et al.			
	4,785,394	11/15/88	Fischer			
	5,083,260	01/21/92	Tsuchiya			
	4,954,987	09/04/90	Auvinen et al.			
	4,675,850	06/23/87	Kumanoya et al.			
	4,788,667	11/29/88	Nakano et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	M. Bazes et. al., "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. 18 No. 2, pp. 164-172 (Apr. 1983)
	A. Agarwal, "An Evaluation of Directory Schemes for Cache Coherence", IEEE document pp.280-289 (1988)
	K. Numata et. al. " New Nibbled-Page Architecture for High Density DRAM's", IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 900-904 (Aug. 1989)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,633,735	05/05/87	Novak, et. al			
	4,672,470	06/09/87	Morimoto, et. al			
	4,719,505	01/12/88	Katznelson			
	4,825,287	04/25/89	Baji, et. al			
	4,845,677	07/04/89	Chappell, et. al			
	4,873,671	10/10/89	Kowshik, et. al			
	4,876,670	10/24/89	Nakabayashi, et. al			
	4,901,036	02/13/90	Herold, et. al			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
	EP 0218523	05/30/89	EPO				
	EP 0282735	09/21/88	EPO				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Horowitz et al., "**MIPS-X: A 20-MIPS Peak 32-Bit Microprocessor with ON-Chip Cache**", IEEE J. Solid State Circuits, vol. SC-22, No. 5, pp. 790-798 (Oct. 1987)
	Robert J. Lodi et al., "**Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit,**" 1976 IEEE International Solid-State Circuits Conference (Feb. 18, 1976)

EXAMINER	DATE CONSIDERED
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,979,145	12/18/90	Remington, et. al			
	5,009,481	04/23/91	Kinoshita, et. al			
	5,016,226	05/14/91	Hiwada, et. al			
	5,036,495	07/30/91	Busch, et. al			
	5,111,486	05/05/92	Oliboni, et. al			
	5,123,100	06/16/92	Hisada, et. al			
	5,142,376	08/25/92	Ogura			
	5,276,846	01/04/94	Aichelmann Jr., et. al			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Whiteside, Frank, "**A Dual-Port 65ns 64Kx4 DRAM with a 50MHz Serial Output,**" IEEE International Solid-State Circuits Conference Digest (Feb. 1986)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	5,301, 278	04/05/95	Bowater, et. al			
	5,361,277	11/01/94	Grover			
	5,684,753	11/04/97	Hashimoto, et al			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
	WO 89/12936	12/28/89	PCT				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Pinkham, Raymond, "**A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications**," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 6, pp. 999-1007 (Dec. 1984)
	Ishimoto, S. et al., "**A 256K Dual Port Memory**," ISSCC Digest of Technical Papers, p. 38-39 (Feb. 1985)
	Iqbal, Mohammad Shakaib, "**Internally Timed RAMs Build Fast Writable Control Stores**," Electronic Design, pp. 93-96 (August 25, 1988)
	Schnaitter, William M. et al., "**A 0.5-GHz CMOS Digital RF Memory Chip**," IEEE Journal of Solid-State Circuits, vol. SC-21, no. 5, pp. 720-726 (Oct. 1986)
	Bursky, Dave, "**Advanced Self-Timed SRAM Pares Access Time to 5 ns**," Electronic Design, pp. 145-147 (Feb. 22, 1990)
	Tomoji Takada et al., "**A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Memories**," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989)

EXAMINER	DATE CONSIDERED
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,330,852	May 18, 1982	Redwine et al.			
	4,703,418	Oct. 27, 1987	James			
	4,726,021	Feb. 16, 1988	Horiguchi et al.			
	4,870,562	Sept. 26, 1989	Kimoto et al.			
	4,763,249	Aug. 09, 1988	Bomba et al			
	4,394,753	July 19, 1983	Penzel			
	4,785,428	Nov. 15, 1988	Bajwa			
	4,680,738	July 14, 1987	Tam			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
	S56-82961	July 7, 1981	Japan				
	S57-14922	Jan. 26, 1982	Japan				
	Sho 60-80193	May 8, 1983	Japan				
	Sho 60-55459	Mar. 30, 1985	Japan				
	S61-72350	April 14, 1986	Japan				
	S63-142445	June 14, 1988	Japan				
	B63-46864	Sept. 19, 1988	Japan				
	S64-29951	Jan. 31, 1989	Japan				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	3,691,534	09/12/72	Veradi, et. al			
	3,771,145	11/06/73	Wiener			
	4,231,104	10/28/80	St.Clair			
	4,466,127	08/14/84	Ohgishi, et. al			
	4,536,795	08/20/85	Hirota, et. al			
	4,616,268	10/07/86	Shida, et. al			
	4,629,909	12/16/86	Cameron			
	4,631,659	12/23/86	Hayne, et. al			
	4,648,102	03/03/87	Riso, et. al			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
	EP 0424774	05/02/91	EPO				
	EP 0449052	03/29/90	EPO				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Takasugi, A. et al., "**A Data-Transfer Architecture for Fast Multi-Bit Serial Acess Mode DRAM**," 11th European Solid State Circuits Conference, Toulouse, France pp.161-165 (Sep. 1985)
	Amitai, Z., "**Burst Mode Memories Improve Cache Design**," WESCON/90 Conference Record, pp. 29-32 (Nov. 1990)
	Ikeda, Hiroaki et al., "**100 MHz Serial Acess Architecture for 4Md Field Memory**," Symposium of VLSI Circuits, Digest of Technical Papers, pp. 11-12 (Jun. 1990)
	Schmitt-Landsiedel, Doris, "**Pipeline Architecture for Fast CMOS Buffer RAMs**," IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, pp. 741-747 (Jun. 1990)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,482,999	11/13/84	Janson et al.			
	4,835,674	05/30/89	Collins et al.			
	5,193,193	03/09/93	Iyer			
	5,179,667	01/12/93	Iyer			
	4,926,385	05/15/90	Fujishima et al.			
	4,566,099	01/21/86	Magerl			
	4,803,621	02/07/89	Kelly			
	4,589,108	05/13/86	Billy			
	4,870,622	09/26/89	Aria et al.			
	5,134,699	07/28/92	Aria et al.			
	4,878,166	10/31/89	Johnson et al.			
	4,849,965	07/18/89	Chomel et al.			
	4,851,990	07/25/89	Johnson et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,048,673	09/13/77	Hendrie et al.			
	4,748,617	05/31/88	Drewlo			
	4,435,762	03/06/84	Milligan et al.			
	4,839,801	06/13/89	Nicely et al.			
	4,949,301	08/14/90	Joshi et al.			
	4,047,246	09/06/77	Kerllenevich et al.			
	5,029,124	07/02/91	Leahy et al.			
	4,625,307	11/25/86	Tulpule et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Watanabe, T.; "Session XIX: High Density SRAMS"; IEEE International Solid State Circuits Conference pp. 266-267 (1987)
	Ohno, C.; "Self-Timed RAM: STRAM"; Fujitsu Sci. TechJ., 24, 4, pp 293-300 (Dec. 1988)
	"Fast Packet Bus for Microprocessor Systems with Caches", IBM Technical Disclosure Bulletin, pp.279-282 (Jan 1989)
	Gustavson, D. "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb 27-Mar 3, 1989)
	James, D.; "Scalable I/O Architecture for Busses"; IEEE, pp. 539-544 (April 1989)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. KA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	5,034,964	Jul. 23, 1991	Khan et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
	SHO 58-192154	Nov. 9, 1983	Japan				
	SHO 63-34795	Feb. 15, 1988	Japan				
	SHO 61-107453	May 26, 1986	Japan				
	SHO 63-91766	April 22, 1988	Japan				
	SHO 62-16289	Jan. 24, 1987	Japan				
	SHO 61-160556	Oct. 4, 1986	Japan				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Robert J. Lodi et al., "**MNOS-BORAM Memory Characteristics,**" IEEE Journal of Solid-State Circuits, vol. SC-11, No. 5, pp. 622-631 (Oct. 1976)
	Gregory Uvieghara et al., "**An On-Chip Smart Memory for a Data-Flow CPU,**" IEEE Journal of Solid-State Circuits, vol. 25, No. 1, pp. 84-89 (Feb. 1990)
	Ray Pinkham et al., "**A 128Kx8 70-MHz Multiport Video RAM with Auto Register Reload and 8x4 WRITE Feature,**" IEEE Journal of Solid State Circuits, vol. 23, no. 3, pp. 1133-1139 (Oct. 1988)
	Hans-Jurgen Mattausch et al., "**A Memory-Based High-Speed Digital Delay Line with a Large Adjustable Length,**" IEEE Journal of Solid-State Circuits, vol. 23, no. 1, pp. 105-110 (Feb. 1988)
	Kanopoulos, Nick and Jill H. Hallenbeck, "**A First-In, First-Out Memory for Signal Processing Applications,**" IEEE Transactions on Circuits and Systems, Vol. CAS-33, No. 5, pp. 556-558 (May 1986)

EXAMINER	DATE CONSIDERED
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified)	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,755,937	July 5, 1989	Glier			
	4,875,192	Oct 17, 1989	Matsumoto			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Pelgrom et al., "A 32-kbit Variable-Length Shift Register for Digital Audio Application", IEEE Journal of Solid-State Circuits, vol. sc-22, no. 3, June 1987, pp 415-422
	Grover et al., "Precision Time-Transfer in Transport Networks Using Digital Crossconnect Systems", IEEE Paper 47.2 Globecom, 1988, pp 1544-1548
	Gustavson et al., "The Scalable Interface Project (Superbus)" (DRAFT), SCI-22 Aug 88-doc1 pp 1-16, August 22, 1988
	Knut Alnes, "SCI: A Proposal for SCI Operation", SCI-10Nov88-doc23, Norsk Data, Oslo, Norway, pp. 1-12, Nov. 10, 1988
	Knut Alnes, "SCI: A Proposal for SCI Operation", SCI-6Jan89-doc31, Norsk Data, Oslo, Norway, pp. 1-24, Jan 6, 1989
	Bakka et al., "SCI: Logical Level Proposals", SCI-6Jan89-doc32, Norsk Data, Oslo, Norway, pp. 1-20, Jan 6, 1989
	Knut Alnes, "Scalable Coherent Interface", SCI-Feb89-doc52, (To appear in Eurobus Conference Proceedings May 1989) pp. 1-8
	Boysel et al., "Four-Phase LSI Logic Offers New Approach to Computer Designer", Four-Phase Systems Inc. Cupertino, CA, Computer Design, April 1970, pp. 141-146,
	Boysel et al., "Random Access MOS Memory Packs More Bits To The Chip", Electronics, Feb. 16, 1970, pp. 109-146

EXAMINER	DATE CONSIDERED
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Hansen et al., "A RISC MICROPROCESSOR WITH INTEGRAL MMU AND CACHE INTERFACE", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 145-148
	Moussouris et al., "A CMOS PROCESSOR WITH INTEGRATED SYSTEMS FUNCTIONS", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 126-130
	"LR2000 High Performance RISC Microprocessor Preliminary" LSI Logic Corp. 1988, pp. 1-15
	"LR2010 Floating Point Accelerator Preliminary" LSI Logic Corp. 1988, pp 1-20
	"High Speed CMOS Databook", Integrated Device Technology Inc. Santa Clara, CA, 1988 pp 9-1 to 9-14
	Riordan T. "MIPS R2000 Processor Interface 78-00005(C)", MIPS Computer Systems, Sunnyvale, CA, June 30, 1987, pp 1-83
	Moussouris, J. "The Advanced Systems Outlook-Life Beyond RISC: The next 30 years in high-performance computing", Computer Letter, July 31, 1989 (an edited excerpt from an address at the fourth annual conference on the Advanced Systems Outlook, in San Francisco, CA (June 5))

EXAMINER	DATE CONSIDERED

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.